

FIG. 1a

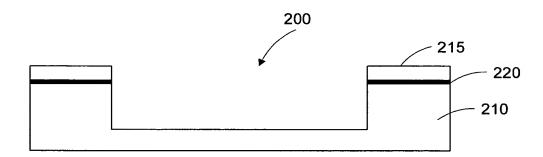


FIG. 1b

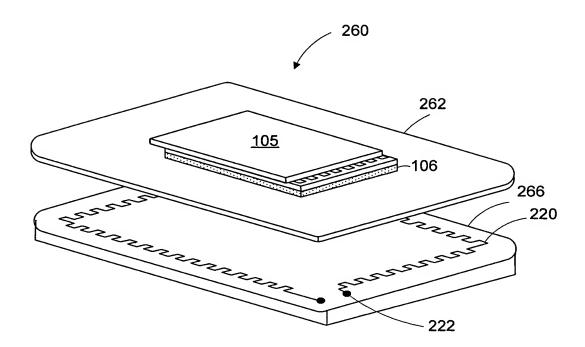
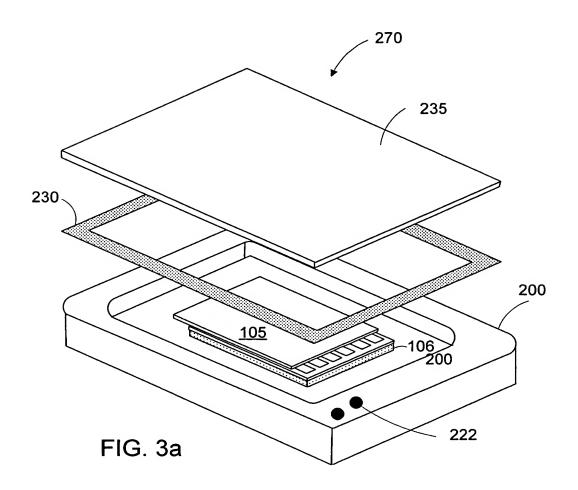


FIG. 2



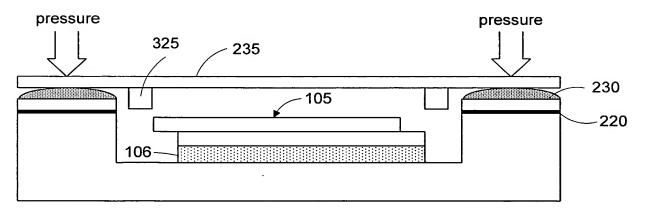
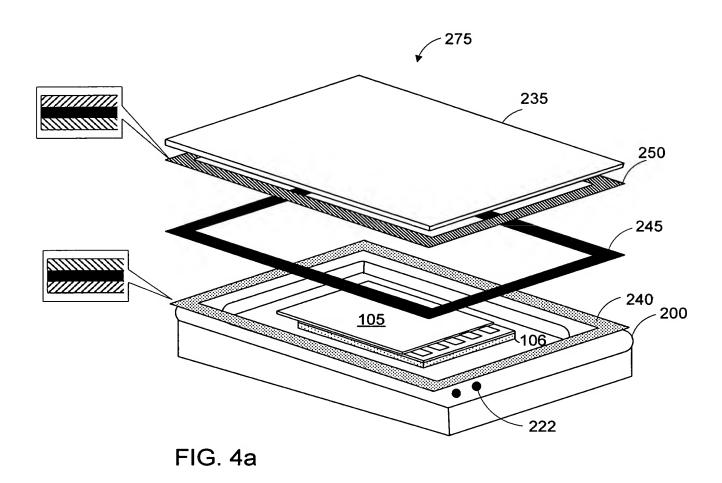


FIG. 3b



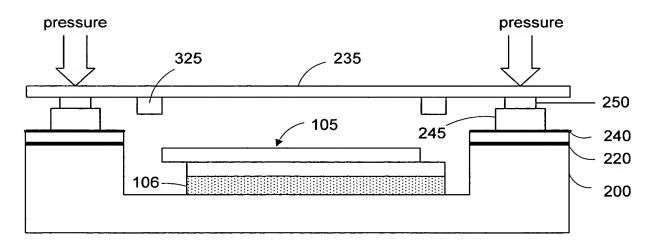


FIG. 4b

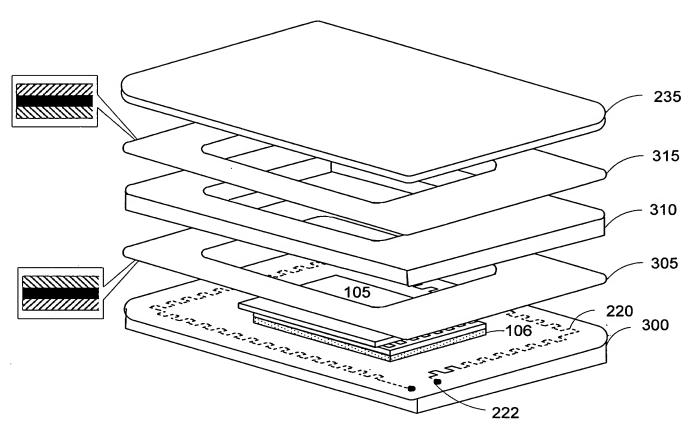


FIG. 5a

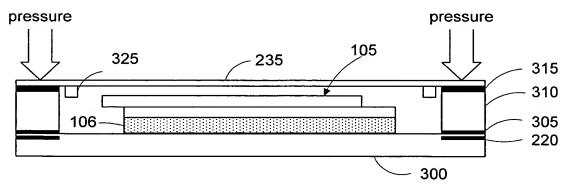


FIG. 5b

## Device Packages with Low Stress Assembly Process P106-US -- Tarn G. Muir 408-737-8100, ext. 136

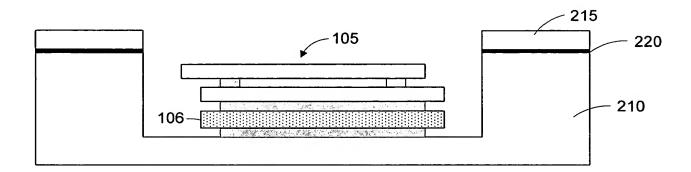


FIG. 6a

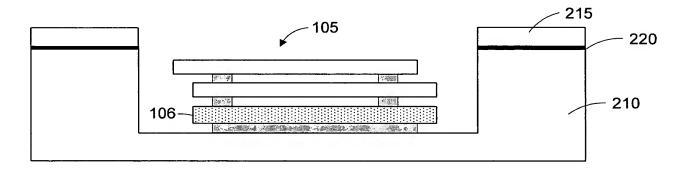


FIG. 6b

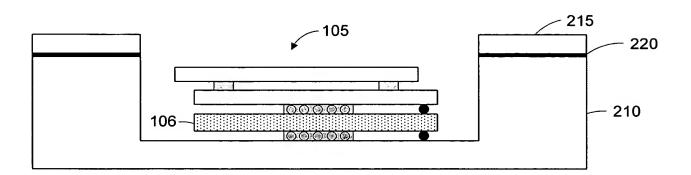


FIG. 6c

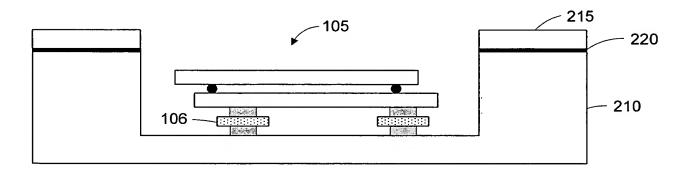


FIG. 6d